UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,809	01/09/2002	Bruce Michael Cassidy	SJO920010074US1 501.396US	5058

7590 05/07/2004

DAVID W. LYNCH
CRAWFORD MAUNU PLLC
1270 NORTHLAND DRIVE, SUITE 390
MENDOTA HEIGHTS, MN 55120

EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	7

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,809	CASSIDY, BRUCE MICHAEL	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-35 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 6-8, 13-15, 20-22, 24-26, 28-30, and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burkhardt, Jr. et al. (5,142,683) (hereinafter Burkhardt) in view of Ogawa et al. (6,237,108) (hereinafter Ogawa).

As to claim 1, Burkhardt teaches a host messaging unit for allowing asynchronous retrieval of a command from a host processor, the host messaging unit comprising: a memory storage device (memory 111); a read controller (service agent 121) coupled to the memory storage device effective to asynchronously retrieve the command from the memory storage device (col. 12, lines 56-68 and col. 13, lines 45-68); and a write controller (service agent 121) coupled to the memory storage device effective to asynchronously acknowledge the command retrieval (erasing the address field 140) (Fig. 6 and col. 13, lines 64-68). However, Burkhardt does not explicitly disclose the host processor is bypassed during both the command retrieval and the asynchronous acknowledgment of the command retrieval. Ogawa teaches DMA controller (21) in a processor module to communicate with a shared memory (col. 11, lines 1-14). It would

have been obvious to one of ordinary skill in the art to implement the read controller and write controller in the system of Burkhardt to be DMA controller so that the host processor is bypassed during both the command retrieval and the asynchronous acknowledgment of the command retrieval as taught by Ogawa to free the processor for other operations.

As to claim 6, Burkhardt further teaches the read controller comprises: a direct memory access read engine (as modified above by Ogawa) coupled to the memory storage device; and a busmaster command engine (logic 65) coupled to the direct memory access read engine to initiate the command retrieval from the memory storage when the busmaster command engine is signaled by the host processor (Figs 4-5 and col. 7, lines 39-65).

As to claim 7, Burkhardt further teaches the busmaster command engine comprises a register (register 80) programmable by the host processor to indicate that the command is available to be retrieved from the memory storage device (note the abstract, col. 7, lines 39-65 and col. 13, lines 59-61).

As to claim 8, Burkhardt teaches a peripheral component interconnect device comprising: a device processor (processor 22); and a host messaging unit coupled to the device processor for facilitating communication between the device processor and an external device (processor 29) (Fig. 6), the host messaging unit including: a read controller (service agent 121) coupled to the device processor effective to asynchronously read a data element (in memory 111) from the external device; and a write controller (service agent 121) coupled to the device processor effective to asynchronously

acknowledge the asynchronous read (erasing the address field 140) (Fig. 6 and col. 13, lines 64-68). However, Burkhardt does not explicitly disclose the host processor is bypassed during both the asynchronous read and the asynchronous acknowledgment of the asynchronous read. Ogawa teaches DMA controller (21) in a processor module to communicate with a shared memory (col. 11, lines 1-14). It would have been obvious to one of ordinary skill in the art to implement the read controller and write controller in the system of Burkhardt to be DMA controller so that the host processor is bypassed during both the asynchronous read and the asynchronous acknowledgment of the asynchronous read as taught by Ogawa to free the processor for other operations.

As to claim 13, Burkhardt further teaches the read controller comprises: a direct memory access read engine (as modified above by Ogawa) coupled to the external device; and a busmaster command engine (logic 65) coupled to the direct memory access read engine to initiate the data element retrieval from the external device when the busmaster command engine is signaled by the external device (Figs 4-5 and col. 7, lines 39-65).

As to claim 14, Burkhardt further teaches the busmaster command engine comprises a register (register 80) programmable by the external device to indicate that the data element is available to be retrieved from the external device (note the abstract, col. 7, lines 39-65 and col. 13, lines 59-61).

As to claim 15, Burkhardt teaches in a computer system, a host processor (processor 29) coupled through a peripheral component interconnect bus (bus 27) to a peripheral component interconnect device (processor 22), the peripheral component

interconnect device comprising: a host messaging unit (logic 65 in Figs. 4-5 and element 117 in Fig. 6) for facilitating communication between the host processor and the peripheral component interconnect device, the host messaging unit including: a read controller (service agent 121) coupled to the host processor effective to asynchronously retrieve host processor commands from the host processor; and a write controller (service agent 121) coupled to the host processor effective to asynchronously acknowledge the command retrieval (erasing the address field 140) (Fig. 6 and col. 13, lines 64-68). However, Burkhardt does not explicitly disclose the host processor is bypassed during both the command retrieval and the asynchronous acknowledgment of the command retrieval. Ogawa teaches DMA controller (21) in a processor module to communicate with a shared memory (col. 11, lines 1-14). It would have been obvious to one of ordinary skill in the art to implement the read controller and write controller in the system of Burkhardt to be DMA controller so that the host processor is bypassed during both the command retrieval and the asynchronous acknowledgment of the command retrieval as taught by Ogawa to free the processor for other operations.

As to claim 20, Burkhardt further teaches the read controller comprises: a direct memory access read engine (as modified above by Ogawa) coupled to the host processor; and a busmaster command engine (logic 65) coupled to the direct memory access read engine to initiate the command retrieval from the host processor when the busmaster command engine is signaled by the host processor (Figs 4-5 and col. 7, lines 39-65).

As to claim 21, Burkhardt further teaches the busmaster command engine comprises a register (register 80) programmable by the host processor to indicate that the

command is available to be retrieved from the host processor (note the abstract, col. 7, lines 39-65 and col. 13, lines 59-61).

As to claim 22, Burkhardt teaches a method of asynchronously servicing a peripheral component interconnect device comprising: accessing host commands from host memory (memory 111); using the host memory to signal the access of the host commands (erasing the address field 140) (Fig. 6 and col. 13, lines 64-68); and providing status (response available) to the host processor after execution of the host commands (col. 14, lines 57-68). However, Burkhardt does not explicitly disclose bypassing the host processor to access host memory. Ogawa teaches DMA controller (21) in a processor module to communicate with a shared memory (col. 11, lines 1-14). It would have been obvious to one of ordinary skill in the art to implement the read controller and write controller in the system of Burkhardt to be DMA controller so that the host processor is bypassed during accessing the memory as taught by Ogawa in the system of Burkhardt to free the processor for other operations.

As to claim 24, Burkhardt further teaches using the host memory to signal the access of the host commands comprises writing zero valued data to the host memory containing the host commands (erasing the address field 140) (Fig. 6 and col. 13, lines 64-68).

As to claim 25, Burkhardt further teaches providing status to the host processor is interrupt driven (col. 13, lines 59-63).

As to claim 26, Burkhardt further teaches the interrupt driven status uses an interrupt pin to notify the host processor (the stages of the register are connected to the

associated interrupt input of the other processor) (note the abstract and col. 7, lines 39-64).

As to claim 28, Burkhardt further teaches bypassing the host processor comprises: allowing the host processor to write the host commands to the host memory; and interrupting the peripheral component interconnect device when the host commands are available in the host memory (col. 13, lines 52-68).

As to claim 29, Burkhardt further teaches interrupting the peripheral component interconnect device comprises writing a logic value to a register (register 80) within the peripheral component interconnect device (col. 7, lines 39-64).

As to claim 30, Burkhardt teaches a method of bus transfer between a host processor (processor 29) and a peripheral component interconnect device processor (processor 22) comprising: writing host processor commands (by client agent 115) to a memory storage device (memory 111); signaling the existence of the host processor commands; and accessing the host processor commands (by service agent 121) from the memory storage device (Fig. 6 and col. 13, lines 52-68). However, Burkhardt does not explicitly disclose bypassing the peripheral component interconnect device processor and the host processor in the step of signaling and accessing. Ogawa teaches DMA controller (21) in a processor module to communicate with a shared memory (col. 11, lines 1-14). It would have been obvious to one of ordinary skill in the art to implement the client agent and the service agent in the system of Burkhardt to be DMA controllers so that the host processors are bypassed during memory related operations as taught by Ogawa in the system of Burkhardt to free the processors for other operations.

As to claim 33, Burkhardt further teaches using a direct memory access read engine (as modified above by Ogawa) to retrieve host processor commands from the memory storage device; and using a direct memory access write engine (as modified above by Ogawa) to signal the host processor that the host processor commands are retrieved (col. 13, lines 52-67).

As to claim 34, Burkhardt teaches an article of manufacture comprising a program storage medium readable by a computer, the medium tangibly embodying one or more programs of instructions executable by the computer to perform a method of bus transfer between a host processor (processor 29) and a peripheral component interconnect device processor (processor 22), the method comprising: writing host processor commands (by client agent 115) to a memory storage device (memory 111); signaling the existence of the host processor commands; and accessing the host processor commands (by service agent 121) from the memory storage device (Fig. 6 and col. 13, lines 52-68). However, Burkhardt does not explicitly disclose bypassing the peripheral component interconnect device processor and the host processor in the step of signaling and accessing. Ogawa teaches DMA controller (21) in a processor module to communicate with a shared memory (col. 11, lines 1-14). It would have been obvious to one of ordinary skill in the art to implement the client agent and the service agent in the system of Burkhardt to be DMA controllers so that the host processors are bypassed during memory related operations as taught by Ogawa in the system of Burkhardt to free the processors for other operations.

As to claim 35, Burkhardt teaches a peripheral component interconnect device comprising: a device processing means (processor 22); and a host messaging unit coupled to the device for facilitating communication between the device processing means and an external device (processor 29) (Fig. 6), the host messaging unit including: a read controller (service agent 121) coupled to the device processing means effective to asynchronously read a data element (in memory 111) from the external device; and a write controller (service agent 121) coupled to the device processing means effective to asynchronously acknowledge the asynchronous read (erasing the address field 140) (Fig. 6 and col. 13, lines 64-68). However, Burkhardt does not explicitly disclose the device processing means is bypassed during both the asynchronous read and the asynchronous acknowledgment of the asynchronous read. Ogawa teaches DMA controller (21) in a processor module to communicate with a shared memory (col. 11, lines 1-14). It would have been obvious to one of ordinary skill in the art to implement the read controller and write controller in the system of Burkhardt to be DMA controller so that the processor is bypassed during both the asynchronous read and the asynchronous acknowledgment of the asynchronous read as taught by Ogawa to free the processor for other operations.

3. Claims 2-3, 5, 9-10, 12, 16-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burkhardt, Jr. et al. (5,142,683) (hereinafter Burkhardt) in view of Ogawa et al. (6,237,108) (hereinafter Ogawa) and further in view of Suh et al. (Pub. No. 2002/0161536) (hereinafter Suh) and Petersen et al. (6,665,673) (hereinafter Petersen).

As to claim 2, the arguments above for claims 1 applies. Burkhardt further teaches the read controller comprises: a direct memory access read engine (as modified above by Ogawa) coupled to the memory storage device (Fig. 6); an interrupt engine to initiate the command retrieval from the memory storage device (col. 13, lines 45-68). However, Burkhardt and Ogawa do not explicitly disclose initiating the command retrieval using a read clock to initiate the retrieval at predetermined intervals, and a validator coupled to the direct memory access read engine to validate the command retrieved from the memory storage device. Suh teaches polling using a clock to initiate polling for data at predetermined interval (paragraphs [0027] and [0040]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement polling at predetermined interval as taught by Suh in the system of Burkhardt and Ogawa to allow flexible accessing to the memory as the intervals can be changed according to the preferences of the service provider (paragraph [0040]). However, Burkhardt, Ogawa, and Suh do not explicitly disclose a validator coupled to the direct memory access read engine to validate the command retrieved from the memory storage device. Petersen teaches a validater (frame invalid molecule) to validate the request retrieval (col. 14, lines 7-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a validater to validate the request retrieval as taught by Peterson in the system of Burkhardt, Ogawa, and Suh to check for invalid commands and thus provide appropriate reaction.

As to claim 3, Suh further teaches the read clock allows programmable predetermined intervals (the periods can be changed according to the preferences of the service provider) (paragraph [0040]).

As to claim 5, Petersen further teaches the validator includes a comparator (checking to see if the count field is zero) to indicate an invalid command when the command is zero valued (col. 14, lines 7-33).

As to claim 9, the arguments above for claims 8 applies. Burkhardt further teaches the read controller comprises: a direct memory access read engine (as modified above by Ogawa) coupled to read the data element from the external device (Fig. 6); an interrupt engine to initiate the data element retrieval from the external device (col. 13, lines 45-68). However, Burkhardt and Ogawa do not explicitly disclose initiating the data element retrieval using a read clock to initiate the retrieval at predetermined intervals, and a validator coupled to the direct memory access read engine to validate the data element retrieved from the external device. Suh teaches polling using a clock to initiate polling for data at predetermined interval (paragraphs [0027] and [0040]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement polling at predetermined interval as taught by Suh in the system of Burkhardt and Ogawa to allow flexible accessing to the data as the intervals can be changed according to the preferences of the service provider (paragraph [0040]). However, Burkhardt, Ogawa, and Suh do not explicitly disclose a validator coupled to the direct memory access read engine to validate the data element retrieved from the external device. Petersen teaches a validater (frame invalid molecule) to validate the request

retrieval (col. 14, lines 7-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a validater to validate the request retrieval as taught by Peterson in the system of Burkhardt, Ogawa, and Suh to check for invalid commands and thus provide appropriate reaction.

As to claim 10, Suh further teaches the read clock allows programmable predetermined intervals (the periods can be changed according to the preferences of the service provider) (paragraph [0040]).

As to claim 12, Petersen further teaches the validator includes a comparator (checking to see if the count field is zero) to indicate an invalid data element when the data element is zero valued (col. 14, lines 7-33).

As to claim 16, the arguments above for claims 15 applies. Burkhardt further teaches the read controller comprises: a direct memory access read engine (as modified above by Ogawa) coupled to the host processor (Fig. 6); an interrupt engine to initiate the command retrieval from the host processor (col. 13, lines 45-68). However, Burkhardt and Ogawa do not explicitly disclose initiating the command retrieval using a read clock to initiate the retrieval at predetermined intervals, and a validator coupled to the direct memory access read engine to validate the command retrieved from the host processor. Suh teaches polling using a clock to initiate polling for data at predetermined interval (paragraphs [0027] and [0040]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement polling at predetermined interval as taught by Suh in the system of Burkhardt and Ogawa to allow flexible accessing to the memory as the intervals can be changed according to the preferences of the service

provider (paragraph [0040]). However, Burkhardt, Ogawa, and Suh do not explicitly disclose a validator coupled to the direct memory access read engine to validate the command retrieved from the host processor. Petersen teaches a validater (frame invalid molecule) to validate the request retrieval (col. 14, lines 7-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a validater to validate the request retrieval as taught by Peterson in the system of Burkhardt, Ogawa, and Suh to check for invalid commands and thus provide appropriate reaction.

As to claim 17, Suh further teaches the read clock allows programmable predetermined intervals (the periods can be changed according to the preferences of the service provider) (paragraph [0040]).

As to claim 19, Petersen further teaches the validator includes a comparator (checking to see if the count field is zero) to indicate an invalid command when the command is zero valued (col. 14, lines 7-33).

4. Claims 4, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burkhardt, Jr. et al. (5,142,683) (hereinafter Burkhardt) in view of Ogawa et al. (6,237,108) (hereinafter Ogawa), Suh et al. (Pub. No. 2002/0161536) (hereinafter Suh) and Petersen et al. (6,665,673) (hereinafter Petersen), and further in view of Urui et al. (JP 61196613) (herein after Urui).

As to claim 4, the argument above for claim 3 applies. However, Burkhardt, Ogawa, and Suh do not explicitly disclose restarting the predetermined interval after the

command retrieval from the memory storage device. Urui teaches restarting the interval after the retrieval from the memory (polling the memory at a required time the data to be received is read (note the abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include restarting the interval after the retrieval from the memory as taught by Urui in the system of Burkhardt, Ogawa, and Suh to avoid continuous polling where the reads in one poll might take greater than or approximately the same time with the predetermined interval.

As to claim 11, the argument above for claim 10 applies. However, Burkhardt, Ogawa, and Suh do not explicitly disclose restarting the predetermined interval after the data element retrieval from the external device. Urui teaches restarting the interval after the retrieval from the memory (polling the memory at a required time the data to be received is read (note the abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include restarting the interval after the retrieval from the memory as taught by Urui in the system of Burkhardt, Ogawa, and Suh to avoid continuous polling where the reads in one poll might take greater than or approximately the same time with the predetermined interval.

As to claim 18, the argument above for claim 17 applies. However, Burkhardt, Ogawa, and Suh do not explicitly disclose restarting the predetermined interval after the command retrieval from the host processor. Urui teaches restarting the interval after the retrieval from the memory (polling the memory at a required time the data to be received is read (note the abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include restarting the interval after the retrieval as

taught by Urui in the system of Burkhardt, Ogawa, and Suh to avoid continuous polling where the reads in one poll might take greater than or approximately the same time with the predetermined interval.

5. Claims 23 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burkhardt, Jr. et al. (5,142,683) (hereinafter Burkhardt) in view of Ogawa et al. (6,237,108) (hereinafter Ogawa) and further in view of Suh et al. (Pub. No. 2002/0161536) (hereinafter Suh).

As to claim 23, the argument above for claim 22 applies. Burkhardt as modified above by Ogawa further teaches allowing the host processor to write the host commands to the host memory (col. 13, lines 45-63) and retrieving valid host commands via interrupt (col. 13, lines 45-68). However Burkhardt and Ogawa do not explicitly disclose retrieving the valid host commands via polling the host memory for valid host commands at predetermined intervals. Suh teaches polling for data at predetermined intervals (paragraphs [0027] and [0040]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement polling for data at predetermined intervals as taught by Suh in the system of Burkhardt and Ogawa to allow flexible accessing to the memory as the intervals can be changed according to the preferences of the service provider (paragraph [0040]).

As to claim 31, the argument above for claim 30 applies. Burkhardt further teaches retrieving host processor commands via interrupt (col. 13, lines 45-68). However Burkhardt and Ogawa do not explicitly disclose retrieving the valid host commands via polling for host processor commands at predetermined intervals. Suh teaches polling for

data at predetermined intervals (paragraphs [0027] and [0040]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement polling for data at predetermined intervals as taught by Suh in the system of Burkhardt and Ogawa to allow flexible accessing to the memory as the intervals can be changed according to the preferences of the service provider (paragraph [0040]).

As to claim 32, Burkhardt further teaches interrupting the host messaging unit when the host commands are available in the memory storage device (col. 13, lines 52-68).

6. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burkhardt, Jr. et al. (5,142,683) (hereinafter Burkhardt) in view of Ogawa et al. (6,237,108) (hereinafter Ogawa) and further in view of Lai et al. (Pub. No. 2001/0032287) (hereinafter Lai).

As to claim 27, the argument above for claim 25 applies. However, Burkhardt and Ogawa do not explicitly disclose the interrupt driven status uses message signaled interrupts to notify the host processor. Lai teaches using message signaled interrupt to reduce the interrupt pins (paragraph [0013]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement message signaled interrupts as taught by Lai in the system of Burkhardt and Ogawa to reduce the interrupt pins.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses exchanging commands/messages using common memory:

US Patent	6,055,579	Goyal et al.
US Patent	5,584,010	Kawai et al.
US Patent	5,617,537	Yamada et al.
US Patent	5,822,421	Ryu
US Patent	5,446,841	Kitano et al.
US Patent	4,862,350	Orr et al.
US Patent	6,131,113	Ellsworth et al.
US Pub. No.	2001/0023467	Fishler et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER